Design Considerations of a 3.1 - 3.5 GHz GaAs FET Feedback Amplifier*

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Abstract

Recent GaAs FET devices have exhibited promising capabilities for microwave amplification. Circuit designers, however, found two problems with the FET applications, namely, the characteristically high input/output impedances are difficult to match into a 50Ω system and the potential instabilities that exists at frequencies below 4 GHz. This paper describes development work done on feedback circuits in designing an unconditionally stable FET amplifier in the 3.1 - 3.5 GHz frequency range by using conventional microstrip techniques, and also investigates the effect of feedback components on noise and output capabilities.

Discussion

GaAs FET's have already demonstrated superior performance when compared to bipolar transistors in microwave amplifier applications. FET's have been reported with F_{max} in excess of 30 GHz; a typical device[1] has G_{max} = 11 dB and NF of 3 dB at 4 GHz also G_{max} = 7 dB and NF of 4 dB at 8 GHz. To date, these devices have been in the laboratory stage but the trend is rapidly changing and within a short time, they should represent a significant portion of the microwave amplifier market.

Scattering parameters of a typical Fairchild GaAs FET are shown in Table 1. When compared with bipolar transistors, up to frequencies of 3 GHz the bipolar transistors offer competitive performance with the exception of output capabilities (now shown). At the higher frequencies the FET has a clear-cut advantage. Note in Table 1 that the 50 ohm transducer gain, $|S_{21}|$, of the FET is typically near unity while $|S_{11}|$ and $|S_{22}|$ are less than one indicating that the device has sufficient gain capabilities but only under matched conditions. The high input/output impedance of the FET represents a difficult problem when matching the device into 50 ohm using distributed transmission line components. In addition, at frequencies below 4 GHz the device is potentially unstable, requiring some lossy circuit element for stabilization. If the stabilizing element, which is typically a resistor, is applied in form of feedback rather than a shunt admittance at the input or output, the losses can be minimized for complete stability.

Historically, microwave amplifier designers could not apply negative feedback in their circuits due to the excessive phase shift caused by the transistors at these frequencies and also because the devices did not have any extra gain margin to sacrifice for feedback. The GaAs FET's opened a new era since the 30 GHz F_{max} capability assures favorable phase characteristics for parallel feedback in S-band with the following results.

1. The device is unconditionally stable; simultaneous conjugate match can be easily computed.
2. The input/output impedances of the device will be lowered which now makes impedance matching an easier task in general. Specifically the transmission line impedances required can be realized in conventional microstrip form.
3. Feedback reduces the effect of device parameter changes on the over-all circuit. This is particularly important in a reactively matched circuit where the impedances of the devices may vary significantly from unit to unit.
4. Since the amplifier's gain comes primarily by eliminating the existing large mismatches at the input and output of the FET, lowering the impedances will also lower the added gain contribution caused by matching the device. A compromise usually will result, selecting feedback such that the device will be unconditionally stable but still has sufficient gain.
5. The feedback resistor adds noise to the input circuit and effectively increases the over-all noise figure of the circuit depending on the value of the resistor. The contribution may however by very small for stages other than the input stage when several stages are cascaded.
6. Feedback reduces the reverse isolation. However, if the amplifier is built by two stage "gain blocks" the isolation of the two cascaded stages is greater than 30dB which is more than sufficient for practical purposes.

Figures 1 and 2 show the location of the stability circles on the input and output plane for the FET with and without feedback at 3 GHz. (Rf is 2500 ohm that proved to be a good practical value) The inside of the circles represent the region of terminations that make the magnitude of the input or output reflection coefficients greater than one. The locations of the center of the stability circles[2] on a unit radius Smith Chart are given by:

$$C_1 = \frac{(S_{ii} - (S_{11}S_{22} - S_{12}S_{21})S_{jj}^*)^*}{|S_{ii}|^2 - |S_{11}S_{22} - S_{12}S_{21}|^2}$$

and the radius of circles:

$$r_1 = \frac{|S_{12}S_{21}|}{|S_{ii}|^2 - |S_{11}S_{22} - S_{12}S_{21}|^2}$$

where i = 1; j = 2 for the input plane

i = 2; j = 1 for the output plane

The 2500 ohm shunt feedback reduces MAG of the device to about 9 dB and the magnitudes of the reflection coefficients to .8 (see Figures 3 and 4). The corresponding stability (k) factor is 1.2 that indicates unconditional stability. Two stages can now be cascaded with relatively simple matching networks where the highest microstrip transmission line impedance is 120 ohm.

The design goal was to have stable 15 dB "gain

blocks" with 50 ohm input and output impedances. In a future design, the same approach will be expanded to cover an octave range from 2 to 4 GHz. The r.f. circuit of the amplifier is shown in Figure 5 and the computer-design response of the circuit is shown in Table 2.

The circuit was constructed on .050" thick highly polished alumina substrate, using pre-tested FET's in flip-chip carriers. At the time of submitting this paper, the first prototypes showed promising correlation between predicted and measured performance in the frequency domain, with the exception of gain which consistently read about 1.5 dB below the design value. Improvement in substrate grounding techniques, however, is expected to increase the gain. Noise figure at 3.1 GHz measured 4.5 dB which is 1.5 dB above the device noise figure when driven by an optimum noise source. The final design of the amplifier will simultaneously optimize noise source impedance and input impedance match so that an improvement in noise figure can reasonably be expected.

Since the optimum noise performance of the FET occurs around 10 mA drain current, the device has greater dynamic range than low-noise bipolar transistors which usually yield optimum noise around 3-5 mA collector current. The two stage gain block has a linear output power in excess of +10 dBm at 3.5 GHz.

The circuit was designed using Fairchild's microwave circuit analysis and optimization routine[6] (soon to be available on the GE timeshare system), based on scattering parameters. The program also provides stability mapping information that was used in achieving the unconditional stability of the amplifier.

Acknowledgements

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References

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2. R. W. Anderson, "S-Parameter Techniques for Faster, More Accurate Network Design", H.P. Journal, Febr. 1967.

3. P. Bodharamik, L. Besser, R. W. Newcomb, "Two Scattering Matrix Programs for Active Circuit Analysis", IEEE Trans. on CT., Nov. 1971.

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S--MAGN AND ANGLES:

FREQ	11		21		12		22	
2000.0	.924	-20.5	1.184	148.7	.043	81.7	.907	-3.8
2500.0	.892	-26.4	1.265	144.0	.051	81.0	.902	-6.1
3000.0	.848	-30.6	1.269	136.0	.059	78.0	.892	-5.9
3500.0	.797	-35.7	1.250	130.8	.064	79.6	.875	-7.0
4000.0	.774	-38.9	1.288	124.4	.068	80.7	.888	-5.8

FREQ	H21	FT	S21	GMS	GMA	K	U	FMAX
2000.0	11.63	7.63	1.46	14.39		.502	20.79	21.92
2500.0	10.20	8.09	2.04	13.92		.500	24.16	40.37
3000.0	9.07	8.52	2.07	13.29		.676	18.40	24.96
3500.0	7.81	8.60	1.94	12.89		.775	17.91	27.51
4000.0	7.36	9.33	2.20	12.77		.765	23.15	57.49

Table 1. Parameters of the FET in flip-chip carrier.

* * * ØVERALL S PARAMETERS * * *

FREQ.	S21	S11		S12		S21		S22		K
MHZ	(DB)	MAG	ANGLE	MAG	ANGLE	MAG	ANGLE	MAG	ANGLE	FACTR
2000.0	-12.04	0.96/	9.0	0.001/	170.3	0.25/	23.0	0.92/	-3.4	24.96
2500.0	-0.35	0.89/	-18.0	0.005/	145.2	0.96/	-9.3	0.85/	-30.1	6.77
3000.0	15.39	0.20/	-90.5	0.030/	55.5	5.88/	-104.8	0.19/	-103.2	2.74
3500.0	14.78	0.24/	73.6	0.032/	-69.5	5.48/	115.3	0.22/	62.2	2.64
4000.0	7.64	0.64/	55.3	0.018/	-159.6	2.41/	10.8	0.46/	58.0	5.43

Table 2. Design s-parameters of the two-stage amplifier.

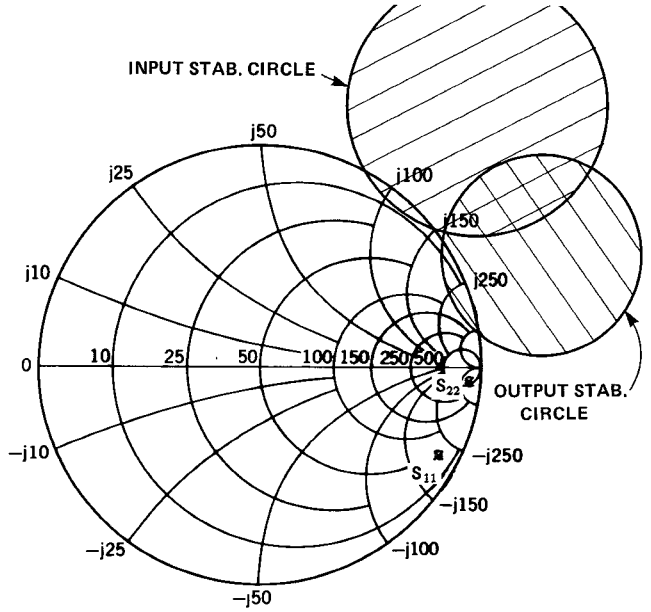

FIG. 1. STABILITY CIRCLES FOR THE FET WITHOUT FEEDBACK

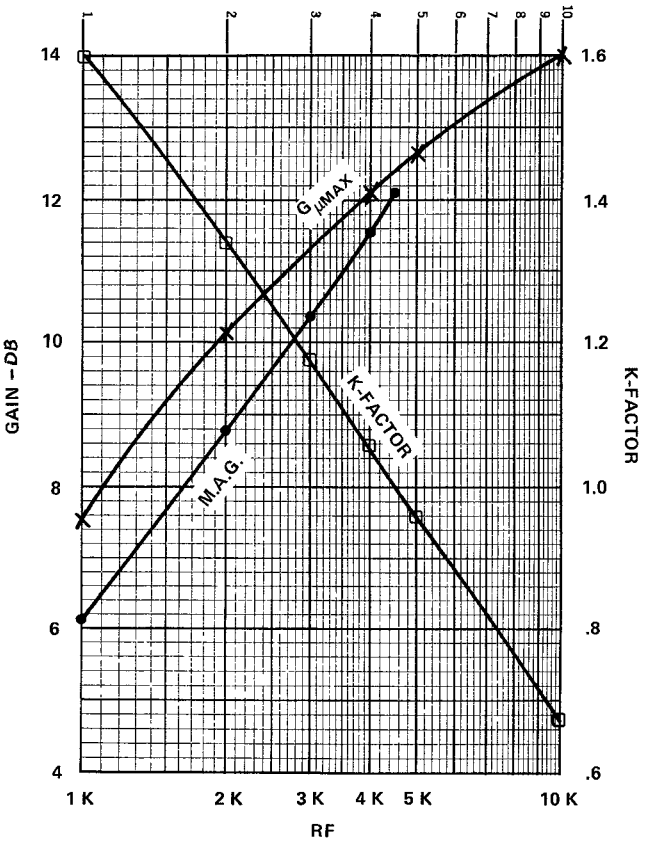

FIG. 3. GAIN AND STABILITY VS. FEEDBACK RESISTANCE

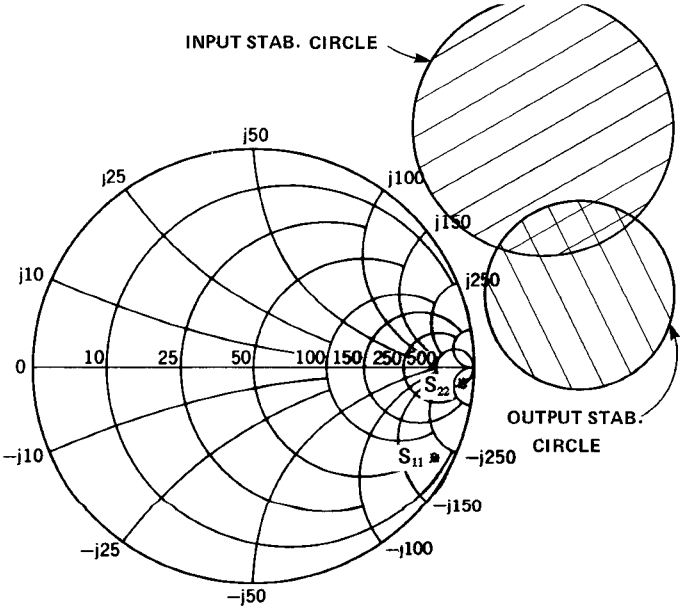

FIG. 2. STABILITY CIRCLES FOR THE FET WITH FEEDBACK

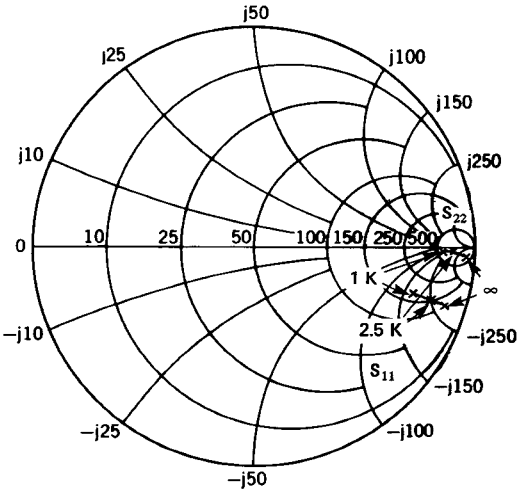

FIG. 4. S_{11} AND S_{22} VS. FEEDBACK RESISTANCE

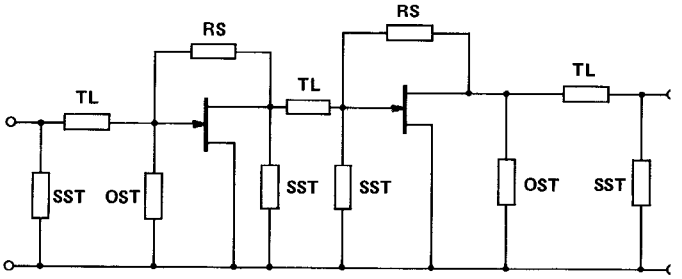

FIG. 5. RF EQUIVALENT CIRCUIT OF THE 3.1–3.5 GHz 2-STAGE AMPLIFIER